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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JIMMIE EARL DEWITT JR., FRANK ELIOT LEVINE,
CHRISTOPHER MICHAEL RICHARDSON,
and ROBERT JOHN URQUHART

Appeal 2008-004152
Application 10/757,212
Technology Center 2100

Decided:[1] July 7, 2009

Before LANCE LEONARD BARRY, HOWARD B. BLANKENSHIP, and STEPHEN C. SIU, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Data (electronic delivery).

STATEMENT OF THE CASE

The Patent Examiner rejected claims 1-23. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

INVENTION

The invention at issue on appeal employs an arithmetic combination of counter values to determine whether to send an interrupt to an interrupt handler of a monitoring application. More specifically, a performance monitoring unit periodically checks the counter values and combines them arithmetically to determine whether a condition exists requiring an interrupt to be sent to the monitoring application. (Spec. 81.)

ILLUSTRATIVE CLAIM

> 1. A method in a data processing system for processing instructions, the method comprising:
>
> receiving a threshold value and an identification of a plurality of addresses to be monitored during the execution of a computer program;
>
> associating hardware counters with the plurality of addresses;
>
> executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered; and
>
> performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present.

PRIOR ART

Levine et al.	5,797,019	Aug. 18, 1998
Burrows	5,887,159	Mar. 23, 1999
Pekarich et al.	6,549,998 B1	Apr. 5, 2003
Bartfai et al.	2003/0101367 A1	May 29, 2003

IBM, *Hardware Cycle Based Memory Residency*, pp. 1-2 (May 22, 2003), available at http://www.priorartdatabase.com/IPCOM/000012728D ("IBMTD").

Randall Hyde, *The Art of Assembly Language* (Linux Edition), pp. 247-248 (2001), available at http://webster.cs.ucr.edu/AoA/Linux/index.html ("Hyde").

REJECTIONS

Claims 1, 2, 4, 8-10, 12, 16-18, 20, and 23 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Pekarich, IBMTD, and Burrows.

Claims 3, 6, 11, 14, 19, and 21 stand rejected under § 103(a) as unpatentable over Pekarich, IBMTD, Burrows, and Levine.

Claims 7, 15, and 22 stand rejected under § 103(a) as unpatentable over Pekarich, IBMTD, Burrows, Levine, and Bartfai.

Claims 5 and 13 stand rejected under § 103(a) as unpatentable over Pekarich, IBMTD, Burrows, and Hyde.

COMBINING TEACHINGS FROM REFERENCES

The Examiner concludes that "it would have been obvious to combine Pekarich, IBMTD, and Burrows" (Answer 6) "to reduce the expense of operations by allowing more immediate and more cost-effective memory management with the use of a hardware cycle counter and PFT cycle counter (IBMTD, pg. 1, paragraph 4, lines 5-7)" (*id.* at 5) and "to measurably improve system performance by making code run faster (Burrows, col. 6, lines 16-20)" (*id.* at 6). The Appellants argue that "the only teaching or suggestion to even attempt the alleged combination is based on a prior knowledge of Appellants' claimed invention thereby constituting impermissible hindsight reconstruction using Appellants' own disclosure as a guide." (Br. 21.)

ISSUE

Therefore, the issue before us is whether the Appellants have shown error in the Examiner's reasons for combining teachings from Pekarich, IBMTD, and Burrows.

LAW

The presence or absence of a reason "to combine references in an obviousness determination is a pure question of fact." *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). "On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary

indicia of nonobviousness." *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998) (citing *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992)).

ANALYSIS

As aforementioned, the Examiner has found reasons for combining teachings from Pekarich, IBMTD, and Burrows. Contrary to the Appellants' argument that "the only teaching or suggestion to even attempt the alleged combination is based on a prior knowledge of Appellants' claimed invention" (Br. 21), the Examiner's reasons are drawn from teachings of the references themselves. The Appellants have not offered any evidence to rebut these findings.

CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Appellants have shown no error in the Examiner's reasons for combining teachings from Pekarich, IBMTD, and Burrows.

TEACHINGS OF BURROWS AND IBMTD

> When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone. Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.

37 C.F.R. § 41.37(c)(1)(vii).

Here, the Appellants argue claims 1, 2, 4, 9, 10, 12, 17, 18, and 20, which are subject to the same ground of rejection, as a first group. (Br. 15-21.) Rather than arguing the rejection of claims 3, 5-7, 11, 13-15, 19, 21, and 22 separately, they rely on their arguments for the group. (*Id.* at 22-24.) We select claim 1 as the sole claim on which to decide the appeal of the first group.

The Appellants also argue claims 8, 16, and 23, which are subject to the same ground of rejection, as a second group. (*Id.* at 22.) We select claim 8 as the sole claim on which to decide the appeal of the second group.

The Examiner makes the following findings.

> Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered (col. 5, lines 13-17 and 31-34; Fig. 5, elements 520 and 540). *It should be noted that the "hit field" is analogous to the "hardware counter', a "hit" to an entry in the prediction table" is analogous to an "address access", and the "best_hint field" is analogous to the "performance indicator."*

(Ans. 5.)

> Burrows' hint fields help branch prediction logic of the CPU 190 to determine the address of the next instruction to be fetched. Thus, Burrows' hint field is an indicator of the next instruction to be fetched ("fetching" being an action). Accordingly, Burrows' hint field sufficiently discloses a "performance indicator."

> . . . [B]ecause the Burrows reference is a computer implemented method, any action that occurs during operation, such as incrementing a counter, is accomplished via executing code in a computer program. In view of this fact, Burrows increments (i.e. executing a computer program and incrementing) the hit field (i.e. respective hardware counters) when there is a hit (i.e. addresses are accessed") and the best_hint field associated with the instructions (i.e. a performance indicator associated with the addresses) is accessed (i.e. encountered). It should be noted that the best_hint field is accessed in order for a determination to be made as to whether the current hint field is identical to the best_hint field.

(*Id.* at 21.)

> IBMTD sufficiently discloses subtracting (i.e. arithmetically combining) values of the hardware counters includes combining values in accordance with the subtraction function of the ALU (i.e. a condition) indicated by commands from the CPU (i.e. a performance monitoring application).

(*Id.* at 29.) Regarding claim 1, the Appellants argue that "Burrows teaches that all of the hint fields associated with an address are counted in order to establish a best_hint field, so that the best_hint field may replace the hint field in the instruction. Thus, Burrows counts all of the hint fields and not just the first events." (Br. 19.) Regarding claim 8, they also argue that they "are claiming that the values of the hardware counters are arithmetically combined when a condition indicated by a performance monitoring application is met. Appellants are not claiming a data structure for storing a difference in calculation as alleged by the Office Action." (*Id.* at 22.)

ISSUE

Therefore, the issue before us is whether the Appellants have shown error in the Examiner's findings about what Burrows and IBMTD teach.

LAW

The question of obviousness is "based on underlying factual determinations including . . . what th[e] prior art teaches explicitly and inherently." *In re Zurko*, 258 F.3d 1379, 1383 (Fed. Cir. 2001) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966); *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999); *In re Napier*, 55 F.3d 610, 613 (Fed. Cir. 1995)).

ANALYSIS

As aforementioned, the Examiner has found that Burrows teaches executing a computer program and incrementing respective hardware counters when a plurality of addresses are accessed and a performance indicator associated with the addresses is encountered. He has also found that IBMTD teaches arithmetically combining values of hardware counters by combining values in accordance with a condition indicated by a performance monitoring application. These findings establish a prima facie case of obviousness.

The Appellants have not addressed the Examiner's specific findings. Furthermore, we also agree with the Examiner (Ans. 29) that the relationship argued by the Appellants, viz., combining the values of the hardware

counters "when a condition indicated by a performance monitoring application is met," is not recited in the language of claim 8.

CONCLUSION

Not having addressed the Examiner's specific findings, the Appellants have shown no error therein.

DECISION

We affirm the rejections of claims 1-23.

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc

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